

Migration from TSC80C32/TSC80C52 to TS80C32X2/TS80C52X2

1. Description

Due to market request, to improve specification and to optimize and rationalize the offer of its microcontroller family, Atmel Wireless & Microcontrollers has redesigned the core of its TSC80C32/TSC80C52 microcontroller. This application note compares the SFRs, DC characteristics, AC characteristics between TSC80C32, TSC80C52 and the new TS80C32X2, TS80C52X2. It should be noted also that the new TS80C32X2, TS80C52X2 core includes the programmable clock doubler feature which is described in a specific application note: ANM072.

2. Features Improvement

	TSC80C32/C52	TS80C32X2/C52X2
256b RAM	Yes	Yes
32 I/Os	Yes	Yes
3 16 bit-Timers	Yes	Yes
Timer 2 : Clock Output Mode	No	Yes
Timer 2 : Auto reload Up/Down Mode	No	Yes
6 Interrupt Sources	Yes	Yes
4 priority level interrupt system	No	Yes
Wake up from Power Down by Reset	Yes	Yes
Wake up from Power Down by INT0 & INT1	No	Yes
UART	Yes	Yes
Enhanced UART	No	Yes
Framing error detection	No	Yes
Multi processor communication	No	Yes
X2 Mode	No	Yes
Dual Data Pointer	No	Yes
Power Off Flag	No	Yes
Commercial Temperature	Yes	Yes
Industrial Temperature	Yes	Yes
Asynchronous port reset	No	Yes
Maximum Frequency @ 5V	44 MHz	40 Mhz X1 Mode 60 Mhz eq. X2 Mode
Maximum Frequency @ 3V	16 Mhz	30 MHz X1 Mode 40 MHz eq. X2 Mode

X1 mode is standard mode (12 clocks per instruction)

X2 mode is new mode (6 clocks per instruction)

3. SFR Mapping

Hereafter a SFR mapping comparison table between TSC80C32/C52 and TS80C32 X2/C52X2

TSC80C32/C52 Old Core

PCON Register (Sfr:87h)

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	PD	IDL

Reset Value : 000x 0000b

TS80C32X2/C52X2 New Core

PCON Register (Sfr:87h)

7	6	5	4	3	2	1	0
SMOD 1	SMOD 0	-	POF	GF1	GF0	PD	IDL

Reset Value : 00x1 0000b

Comments : Power On flag , EUART

TSC80C32/C52 Old Core

Reserved Register (Sfr:8Fh)

TS80C32X2/C52X2 New Core

CKCON Register (Sfr:8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Reset Value : xxxx xxx0b

Comments : X2 mode

TSC80C32/C52 Old Core

SCON Register (Sfr:98h)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Reset Value : 0000 0000b

TS80C32X2/C52X2 New Core

SCON Register (Sfr:98h)

7	6	5	4	3	2	1	0
FE/ SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Reset Value : 0000 0000b

Comments : EUART : FE/SM0 Framing Error

TSC80C32/C52 Old Core

Reserved (Sfr:0A2h)

TS80C32X2/C52X2 New Core

AUXR1 Register (Sfr:0A2h)

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Reset Value : xxxx 00x0b

Comments : Dual DPTR

TSC80C32/52 Old Core

Reserved (Sfr:0A9h)

TS80C32X2/C52X2 New Core

SADDR Register (Sfr:0A9h)

7	6	5	4	3	2	1	0

Reset Value : 0000 0000b

Comments : EUART : Multiprocessor communication

TSC80C32/C52 Old Core

Reserved (Sfr:0B7h)

TS80C32X2/C52X2 New Core

IPH Register (Sfr:0B7h)

7	6	5	4	3	2	1	0
-	-	-	PSH	PT1H	PX1H	PT0H	PX0H

Reset Value : xxx0 0000b

Comments : 4 level priority interrupt

TSC80C32/C52 Old Core

Reserved (Sfr:0B9h)

TS80C32X2/C52X2 New Core

SADEN Register (Sfr:0B9h)

7	6	5	4	3	2	1	0

Reset Value : 0000 0000b

Comments : EUART : Multi processor communication

All other registers are identical

4. DC Parameters

TSC80C32/TSC80C52 : $V_{CC} = 5V \pm 10\%$; $T = -40$ to $+85^{\circ}C$; $T=0$ to $70^{\circ}C$

TS80C32X2/TS80C52X2 : $V_{CC} = 5V \pm 10\%$; $T = -40$ to $+85^{\circ}C$; $T=0$ to $70^{\circ}C$

Symbol	Parameters	TSC80C32 TSC80C52		TS80C32X2 TS80C52X2		Unit	Comments
		Min	Max	Min	Max		
VIH	Input High Voltage except XTAL1,RST	$0.2V_{CC}+1.4$		$0.2V_{CC}+0.9$		V	
IPD	Power Down Current		75		50	μA	$V_{CC} = 2.0V$ to $5.5V$

5. AC Parameters

5.1. TS80C32X2/TS80C52X2 (M Version)

5.1.1. External Program Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Mxx TS80C52X2-Mxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{LHLL}	ALE pulse width	Min	110	90	70	115	90	70	ns
t _{AVLL}	Address valid to ALE low	Min	40	30	20	47.5	35	25	ns
t _{LLAX}	Address hold after ALE low	Min	35	35	35	47.5	35	25	ns
t _{LLIV}	ALE low to valid instruction in	Max	185	170	130	220	170	130	ns
t _{LLPL}	ALE low to PSEN low	Min	45	40	30	52.5	40	30	ns
t _{PLPH}	PSEN pulse width	Min	165	130	100	167.5	130	100	ns
t _{PLIV}	PSEN low to valid instruction in	Max	125	110	85	147.5	110	80	ns
t _{PXIX}	input instruction hold after PSEN	Min	0	0	0	0	0	0	ns
t _{PXIZ}	Input instruction float after PSEN	Max	50	45	35	55.5	43	33	ns
t _{AVIV}	Address to valid instruction in	Max	230	210	170	272.5	210	160	ns
t _{PLAZ}	PSEN low to address float	Max	10	10	8	10	10	10	ns

5.1.2. External Data Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Mxx TS80C52X2-Mxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{RLRH}	RD pulse width	Min	340	270	210	355	280	220	ns
t _{WLWH}	WR pulse width	Min	340	270	210	355	280	220	ns
t _{RLDV}	RD Low to valid data in	Max	240	210	175	287.5	225	175	ns
t _{RHDX}	Data hold after RD	Min	0	0	0	0	0	0	ns
t _{RHDZ}	Data float after RD	Max	90	90	80	105	80	60	ns
t _{LLDV}	ALE low to valid data in	Max	435	370	290	460	360	280	ns
t _{AVDV}	Address to valid data in	Max	480	400	320	502.5	390	300	ns
t _{LLWL}	ALE low to RD or WR low	Min	150	135	120	162.5	125	95	ns
t _{LLWL}	ALE low to RD or WR low	Max	250	170	130	212.5	175	145	ns
t _{AVWL}	Address valid to WR low or RD low	Min	180	180	140	225	175	135	ns
t _{QVWX}	Data valid to WR transition	Min	35	35	30	47.5	35	25	ns
t _{WHQX}	Data hold after WR	Min	40	35	30	52.5	40	30	ns
t _{QVWH}	Data valid to to WR High	Min	380	325	250	422.5	335	265	ns
t _{TRLAZ}	RD low to address float	Min	0	0	0	0	0	0	ns
t _{WHLH}	RD or WR high to ALE high	Min	35	35	25	47.5	35	25	ns
t _{WHLH}	RD or WR high to ALE high	Max	90	60	45	77.5	65	55	ns

5.1.3. Serial Port Timing - Shift register

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Mxx TS80C52X2-Mxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{XLXL}	Serial port clock cycle time	Min	750	600	480	750	600	480	ns
t _{QVXH}	Output data setup to clock rising edge	Min	563	480	380	575	450	350	ns
t _{XHQX}	Output data hold after clock edge	Min	63	90	65	105	80	60	ns
t _{XHDX}	Input data hold after clock rising edge	Min	0	0	0	0	0	0	ns
t _{XHDV}	Clock rising edge to input data valid	Max	563	450	350	492	367	267	ns

5.2. TS80C32X2/TS80C52X2 (L Version)

5.2.1. External Program Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Mxx TS80C52X2-Mxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{LHLL}	ALE pulse width	Min	110	90	70	110	85	65	ns
t _{AVLL}	Address valid to ALE low	Min	40	30	20	42.5	30	20	ns
t _{LLAX}	Address hold after ALE low	Min	35	35	35	42.5	30	20	ns
t _{LLIV}	ALE low to valid instruction in	Max	185	170	130	215	165	125	ns
t _{LLPL}	ALE low to PSEN low	Min	45	40	30	47.5	35	25	ns
t _{PLPH}	PSEN pulse width	Min	165	130	100	162.5	125	95	ns
t _{PLIV}	PSEN low to valid instruction in	Max	125	110	85	142.5	105	75	ns
t _{PXIX}	input instruction hold after PSEN	Min	0	0	0	0	0	0	ns
t _{PXIZ}	Input instruction float after PSEN	Max	50	45	35	47.5	35	25	ns
t _{AVIV}	Address to valid instruction in	Max	230	210	170	267.5	205	155	ns
t _{PLAZ}	PSEN low to address float	Max	10	10	8	10	10	10	ns

5.2.2. External Data Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Mxx TS80C52X2-Mxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{RLRH}	RD pulse width	Min	340	270	210	350	275	215	ns
t _{WLWH}	WR pulse width	Min	340	270	210	350	275	215	ns
t _{RLDV}	RD Low to valid data in	Max	240	210	175	282.5	220	170	ns
t _{RHDX}	Data hold after RD	Min	0	0	0	0	0	0	ns
t _{RHDZ}	Data float after RD	Max	90	90	80	100	75	55	ns
t _{LLDV}	ALE low to valid data in	Max	435	370	290	455	355	275	ns
t _{AVDV}	Address to valid data in	Max	480	400	320	497.5	385	295	ns
t _{LLWL}	ALE low to RD or WR low	Min	150	135	120	157.5	120	90	ns
t _{LLWL}	ALE low to RD or WR low	Max	250	170	130	217.5	180	150	ns
t _{AVWL}	Address valid to WR low or RD low	Min	180	180	140	220	170	130	ns
t _{QVWX}	Data valid to WR transition	Min	35	35	30	167.5	130	100	ns
t _{WHQX}	Data hold after WR	Min	40	35	30	42.5	30	20	ns
t _{QVWH}	Data valid to to WR High	Min	380	325	250	417.5	330	260	ns
t _{TRLAZ}	RD low to address float	Min	0	0	0	0	0	0	ns
t _{WHLH}	RD or WR high to ALE high	Min	35	35	25	42.5	30	20	ns
t _{WHLH}	RD or WR high to ALE high	Max	90	60	45	82.5	70	60	ns

5.2.3. Serial Port Timing - Shift register

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-Lxx TS80C52X2-Lxx			Unit
			16 MHz	20 MHz	25 MHz	16 MHz	20 MHz	25 MHz	
t _{XLXL}	Serial port clock cycle time	Min	750	600	480	750	600	480	ns
t _{QVXH}	Output data setup to clock rising edge	Min	563	480	380	575	450	350	ns
t _{XHQX}	Output data hold after clock edge	Min	63	90	65	105	80	60	ns
t _{XHDX}	Input data hold after clock rising edge	Min	0	0	0	0	0	0	ns
t _{XHDV}	Clock rising edge to input data valid	Max	563	450	350	492	367	267	ns

5.3. TS80C32X2/TS80C52X2 (V Version)

5.3.1. External Program Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-V _{xx} TS80C52X2-V _{xx}			Unit
			25 MHz	30 MHz	40 MHz	25 MHz	30 MHz	40 MHz	
t _{LHLL}	ALE pulse width	Min	70	60	40	72	58.7	42.0	ns
t _{AVLL}	Address valid to ALE low	Min	20	15	9	27	20.3	12.0	ns
t _{LLAX}	Address hold after ALE low	Min	35	35	30	27	20.3	12.0	ns
t _{LLIV}	ALE low to valid instruction in	Max	130	100	70	138	111.3	78.0	ns
t _{LLPL}	ALE low to PSEN low	Min	30	25	15	32	25.3	17.0	ns
t _{PLPH}	PSEN pulse width	Min	100	80	65	105	85.0	60.0	ns
t _{PLIV}	PSEN low to valid instruction in	Max	85	65	45	95	75.0	50.0	ns
t _{PXIX}	input instruction hold after PSEN	Min	0	0	0	0	0.0	0.0	ns
t _{PXIZ}	Input instruction float after PSEN	Max	35	30	20	35	28.3	20.0	ns
t _{AVIV}	Address to valid instruction in	Max	170	130	80	170	136.7	95.0	ns
t _{PLAZ}	PSEN low to address float	Max	8	6	5	10	10.0	10.0	ns

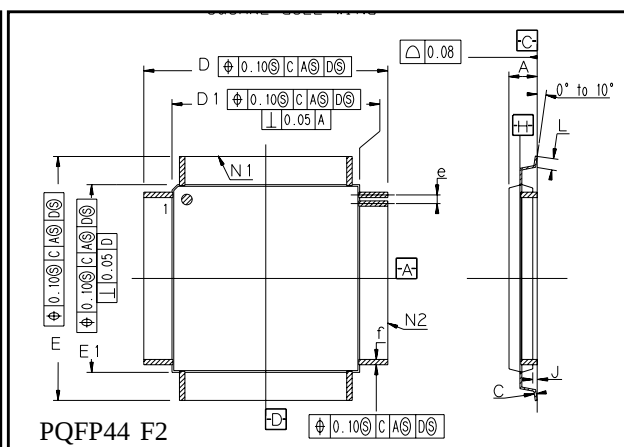
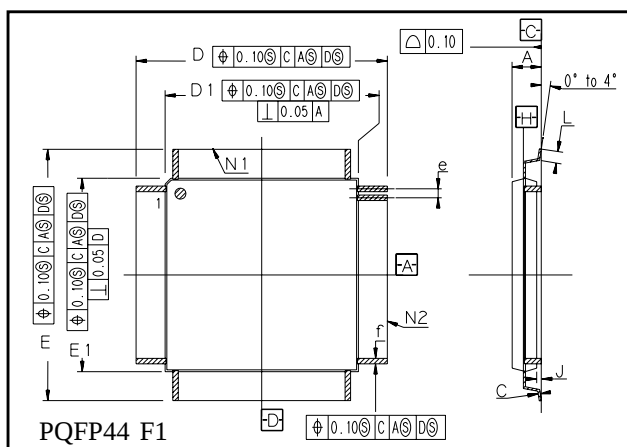
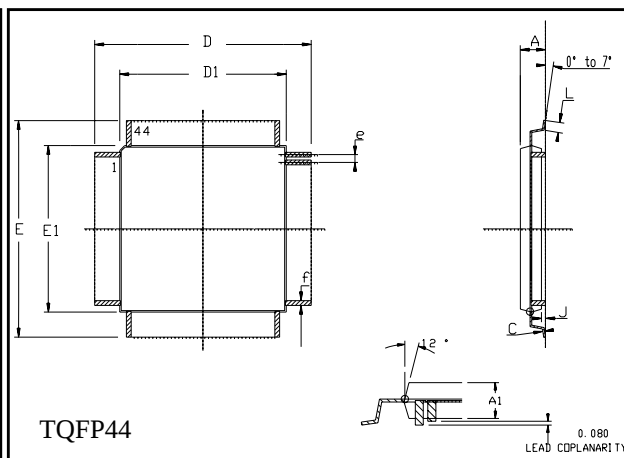
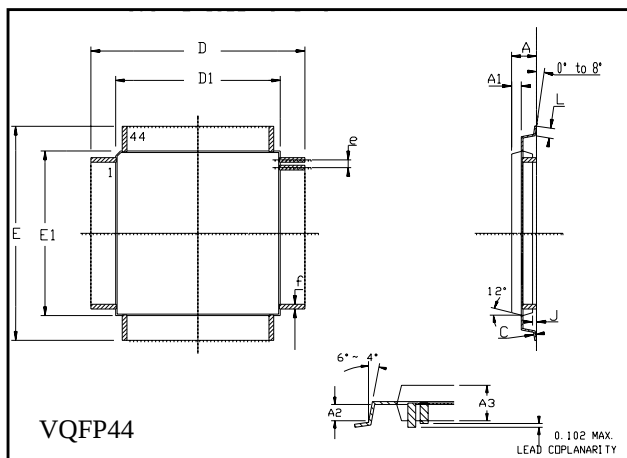
5.3.2. External Data Memory Characteristics

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-V _{xx} TS80C52X2-V _{xx}			Unit
			25 MHz	30 MHz	40 MHz	25 MHz	30 MHz	40 MHz	
t _{RLRH}	RD pulse width	Min	210	180	100	225.0	185.0	135.0	ns
t _{WLWH}	WR pulse width	Min	210	180	100	225.0	185.0	135.0	ns
t _{RLDV}	RD Low to valid data in	Max	175	135	90	177.0	143.7	102.0	ns
t _{RHDX}	Data hold after RD	Min	0	0	0	0.0	0.0	0.0	ns
t _{RHDZ}	Data float after RD	Max	80	70	45	65.0	51.7	35.0	ns
t _{LLDV}	ALE low to valid data in	Max	290	235	150	285.0	231.7	165.0	ns
t _{AVDV}	Address to valid data in	Max	320	260	180	310.0	250.0	175.0	ns
t _{LLWL}	ALE low to RD or WR low	Min	120	90	60	100.0	80.0	55.0	ns
t _{LLWL}	ALE low to RD or WR low	Max	130	115	95	140.0	120.0	95.0	ns
t _{AVWL}	Address valid to WR low or RD low	Min	140	115	65	140.0	113.3	80.0	ns
t _{QVWX}	Data valid to WR transition	Min	30	20	10	52.5	40	30	ns
t _{WHQX}	Data hold after WR	Min	30	20	10	32.0	25.3	17.0	ns
t _{QVWH}	Data valid to to WR High	Min	250	215	160	270.0	223.3	165.0	ns
t _{TRLAZ}	RD low to address float	Min	0	0	0	0.0	0.0	0.0	ns
t _{WHLH}	RD or WR high to ALE high	Min	25	20	15	30.0	23.3	15.0	ns
t _{WHLH}	RD or WR high to ALE high	Max	45	40	35	50.0	43.3	35.0	ns

5.3.3. Serial Port Timing - Shift register

Symbol	Parameter	Cond.	TSC80C32 TSC80C52			TS80C32X2-V _{xx} TS80C52X2-V _{xx}			Unit
			25 MHz	30 MHz	40 MHz	25 MHz	30 MHz	40 MHz	
t _{XLXL}	Serial port clock cycle time	Min	480	400	250	480.0	400.0	300.0	ns
t _{QVXH}	Output data setup to clock rising edge	Min	380	300	170	350.0	283.3	200.0	ns
t _{XHQX}	Output data hold after clock edge	Min	65	50	35	60.0	46.7	30.0	ns
t _{XHDX}	Input data hold after clock rising edge	Min	0	0	0	0.0	0.0	0.0	ns
t _{XHDV}	Clock rising edge to input data valid	Max	350	300	200	267.0	200.3	117.0	ns

6. Packages



		A	C	D	D1	E	E1	e	f	J	L	N1	N2
PQFP44 F2	Min	1.90	0.10	12.10	9.90	12.10	9.90	0.80	0.25	0.00	0.35	11	11
	Max	2.40	0.20	12.50	10.10	12.50	10.10		0.45	0.20	0.65		
PQFP44 F1	Min	2.00	0.10	13.65	9.90	13.65	9.90	0.80	0.20	0.00	0.65	11	11
	Max	2.40	0.20	14.15	10.1	14.15	10.10		0.40	0.30	0.95		
VFQFP44	Min	-	0.10	11.90	9.90	11.90	9.90	0.80	0.35	0.05	0.45	11	11
	Max	1.6	0.20	12.10	10.10	12.10	10.10			-	0.75		
TQFP44	Min	-	0.09	12.00	10.00	12.00	10.00	0.80	0.30	0.05	0.45	11	11
	Max	1.20	0.20						0.45	0.15	0.75		

7. Cross Reference

if -xx stands for -12, -16, -20, -25, -30, -36, -40 then * = -M

if -xx stands for -44, then * = -V, if -xx stands for -L16 or -L20, then * = -L

Old ATMEL part	New ATMEL part	Old ATMEL part	New ATMEL part
P80C32-xx	TS80C32X2-*CA	P80C52-XX	TS80C52X2-*CA
S80C32-xx	TS80C32X2-*CB	S80C52-XX	TS80C52X2-*CB
F180C32-xx	TS80C32X2-*CC	F180C52-XX	TS80C52X2-*CC
F280C32-xx	TS80C32X2-*CE	F280C52-XX	TS80C52X2-*CE
V80C32-xx	TS80C32X2-*CE	V80C52-XX	TS80C52X2-*CE
T80C32-xx	TS80C32X2-*CE	T80C52-XX	TS80C52X2-*CE
D80C32-xx	No equivalent	D80C52-XX	TS80C52X2-*CJ
Q80C32-xx	No equivalent	Q80C52-XX	TS80C52X2-*CK
R80C32-xx	No equivalent	R80C52-XX	No equivalent
IP80C32-xx	TS80C32X2-*IA	IP80C52-XX	TS80C52X2-*IA
IS80C32-xx	TS80C32X2-*IB	IS80C52-XX	TS80C52X2-*IB
IF180C32-xx	TS80C32X2-*IC	IF180C52-XX	TS80C52X2-*IC
IF280C32-xx	TS80C32X2-*IE	IF280C52-XX	TS80C52X2-*IE
IV80C32-xx	TS80C32X2-*IE	IV80C52-XX	TS80C52X2-*IE
IT80C32-xx	TS80C32X2-*IE	IT80C52-XX	TS80C52X2-*IE
ID80C32-xx	No equivalent	ID80C52-XX	TS80C52X2-*IJ
IQ80C32-xx	No equivalent	IQ80C52-XX	TS80C52X2-*IK
IR80C32-xx	No equivalent	IR80C52-XX	No equivalent
P80C32-L16	TS80C32X2-LCA	P80C52-L16	TS80C52X2-LCA
S80C32-L16	TS80C32X2-LCB	S80C52-L16	TS80C52X2-LCB
F180C32-L16	TS80C32X2-LCC	F180C52-L16	TS80C52X2-LCC
F280C32-L16	TS80C32X2-LCE	F280C52-L16	TS80C52X2-LCE
V80C32-L16	TS80C32X2-LCE	V80C52-L16	TS80C52X2-LCE
T80C32-L16	TS80C32X2-LCE	T80C52-L16	TS80C52X2-LCE
D80C32-L16	No equivalent	D80C52-L16	TS80C52X2-LCJ
Q80C32-L16	No equivalent	Q80C52-L16	TS80C52X2-LCK
R80C32-L16	No equivalent	R80C52-L16	No equivalent
IP80C32-L16	TS80C32X2-LIA	IP80C52-L16	TS80C52X2-LIA
IS80C32-L16	TS80C32X2-LIB	IS80C52-L16	TS80C52X2-LIB
IF180C32-L16	TS80C32X2-LIC	IF180C52-L16	TS80C52X2-LIC
IF280C32-L16	TS80C32X2-LIE	IF280C52-L16	TS80C52X2-LIE
IV80C32-L16	TS80C32X2-LIE	IV80C52-L16	TS80C52X2-LIE
IT80C32-L16	TS80C32X2-LIE	IT80C52-L16	TS80C52X2-LIE
ID80C32-L16	No equivalent	ID80C52-L16	TS80C52X2-LIJ
IQ80C32-L16	No equivalent	IQ80C52-L16	TS80C52X2-LIK
IR80C32-L16	No equivalent	IR80C52-L16	No equivalent
AX80C32-xx	No equivalent	AX80C52-XX	No equivalent
MX80C32-xx	No equivalent	MX80C52-XX	No equivalent

8. Bibliography

TSC80C32/TSC80C52 datasheet Rev.H (13 Feb. 97)

TS80C32X2/TS80C52X2/TS87C52X2 datasheet Rev. B (Aug. 31,1999)